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L3 and coil	10

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<u>L5</u>	L3 and coil	10	<u>L5</u>
<u>L4</u>	L3 with modulat\$	6	<u>L4</u>
<u>L3</u>	L2 with (calculat\$ or estimat\$)	146	<u>L3</u>
<u>L2</u>	L1 with signal	2438	<u>L2</u>
<u>L1</u>	average adj current	16456	<u>L1</u>

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AND  in All Fields



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average <phrase> current <and> signal  
<and> calculating




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**Search:**

L8





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<u>L8</u>	L7 and calculat\$	2	<u>L8</u>
<u>L7</u>	L6 and modulat\$	2	<u>L7</u>
<u>L6</u>	L5 and average and current	10	<u>L6</u>
<u>L5</u>	L3 and coil	10	<u>L5</u>
<u>L4</u>	L3 with modulat\$	6	<u>L4</u>
<u>L3</u>	L2 with (calculat\$ or estimat\$)	146	<u>L3</u>
<u>L2</u>	L1 with signal	2438	<u>L2</u>
<u>L1</u>	average adj current	16456	<u>L1</u>

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☐ 1. Document ID: US 6455820 B2

L8: Entry 1 of 2

File: USPT

Sep 24, 2002

US-PAT-NO: 6455820

DOCUMENT-IDENTIFIER: US 6455820 B2

TITLE: Method and apparatus for detecting a dry fire condition in a water heater

DATE-ISSUED: September 24, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Bradenbaugh; Kenneth A.	Concord	OH	44077	

US-CL-CURRENT: 219/481; 219/483, 219/486, 323/235, 374/102

Full	Title	Citation	Front	Review	Classification	Date	Reference	Abstract	Abstract Refs	Claims	RMIC	Draw. Data
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☐ 2. Document ID: US 4656402 A

L8: Entry 2 of 2

File: USPT

Apr 7, 1987

US-PAT-NO: 4656402

DOCUMENT-IDENTIFIER: US 4656402 A

TITLE: Electric motor control apparatus

DATE-ISSUED: April 7, 1987

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Nishikawa; Takayoshi	Chiryu			JP

US-CL-CURRENT: 388/811; 388/907.5, 388/921

Full	Title	Citation	Front	Review	Classification	Date	Reference	Abstract	Abstract Refs	Claims	RMIC	Draw. Data
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» Key

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IET JNL IET Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IET CNF IET Conference Proceeding

IEEE STD IEEE Standard

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 Vlassis, S.; Siskos, S.;  
[Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on Systems I: Regular Papers, IEEE Transactions on](#)  
 Volume 48, Issue 7, July 2001 Page(s):910 - 914  
 Digital Object Identifier 10.1109/81.933335  
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(180 KB\)](#) IEEE JNL  
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- ☐ 2. **CMOS outlier rejection circuit**  
 Vlassis, S.; Siskos, S.;  
[Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IE Symposium on](#)  
 Volume 5, 28-31 May 2000 Page(s):729 - 732 vol.5  
 Digital Object Identifier 10.1109/ISCAS.2000.857605  
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- ☐ 3. **Static electromigration analysis for signal interconnects**  
 Chanhee Oh; Blaauw, D.; Becer, M.; Zolotov, V.; Panda, R.; Dasgupta, A.;  
[Quality Electronic Design, 2003. Proceedings. Fourth International Symposium](#)  
 24-26 March 2003 Page(s):377 - 382  
 Digital Object Identifier 10.1109/ISQED.2003.1194762  
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- ☐ 4. **A new duty cycle parallel control method and FPGA implementation for power factor correction (PFC)**  
 Zhang, W.; Feng, G.; Liu, Y.-F.; Wu, B.;  
[Applied Power Electronics Conference and Exposition, 2005. APEC 2005. Tw](#)  
 Volume 2, 6-10 March 2005 Page(s):805 - 811 Vol. 2  
 Digital Object Identifier 10.1109/APEC.2005.1453072  
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